## REMARKS

Claims 1-36 are finally rejected under 35 U.S.C. ¶ 103 as being unpatentable over Acres et al. in view of IEEE-1394: An Emerging Interconnection System for Future Simulations ("IEEE-1394") and Creating One Industry Standard for Manufactures of Electronic Games of Chance ("Creating One Industry Standard"), all of record. In support of the rejection, the examiner contends that Acres et al. discloses all of the claimed subject matter except for the use of a network which provides power to the interconnected devices, but that the latter feature is taught by IEEE-1394, and that it would have been obvious, in view of the motivation provided by Creating One Industry Standard, to substitute the IEEE-1394 network for the Ethernet network disclosed by Acres et al. The independent claims have been further amended to clarify the patentable distinctions between those claims and the cited art.

A significant aspect of applicants' invention is the provision of a gaming system which includes a four-line or wire interconnection among a host controller and a plurality of local controllers, wherein the four wires provide power to the local controllers, as well as transmitting data from the host controller to the local controllers and/or from the local controllers to the host controller. In order to clarify this point, each of the independent claims 1, 5 and 13 has been amended to specify "the controllers being interconnected with one another by no more than four lines including a data line, a power line, a common line and a return line," and to further specify "the return line interconnecting all of the local controllers with the host controller." The power line interconnects power terminals of all of the controllers and the common line interconnects common terminals of all of the controllers. No such arrangement is disclosed or suggested by the cited art.

The elements of the Acres et al. system are interconnected over an industry standard Ethernet network (Col. 7, lines 45-49). That Ethernet network does not supply power and ground to the devices on the network, nor is there any need to provide power or ground to the control devices of the Acres et al. network, since the devices are gaming machines, each of which will be powered locally. In applicants' disclosed invention, on the other hand, the provision of power and ground connections to each of the accessed devices is important, since these devices may be devices such as switches or lamps within an individual gaming machine.

The examiner acknowledges this deficiency in Acres et al., but contends that it is supplied by IEEE-1394, which discloses a connection standard utilizing six wires or conductors, including two twisted pairs for data transport and synchronization and one pair for power distribution (IEEE-1394, pg. 4, first paragraph and Fig. 10). While the reference discloses that it is possible to utilize a four-conductor cable, that configuration "eliminates the power distribution cables" (pg. 4, first paragraph). Thus, IEEE-1394 does not disclose a four-line interconnection including a power line and a common line. Accordingly, even if one were motivated to attempt to combine the teachings of Acres et al. and IEEE-1394 in the manner suggested by the examiner, such a combination would not result in the invention recited in amended claims 1, 5 and 13 and the claims dependent thereon.

Another significant aspect of applicants' invention is that it is a position-based system rather than an addressable system. In other words, each of the "plurality of devices" to be individually accessed corresponds to a particular position in a shift register formed by the local controllers, and each one of those positions contains a

single bit from the host controller. Thus, the particular device which will be controlled by any particular bit of the data stream is governed by that bit's position in the shift register after the data word is loaded into the shift register. In both Ethernet and the IEEE-1394 systems, on the other hand, particular devices in the network are designated by addresses assigned to those devices. This feature is spelled out in claims 13, 24 and 31, which have been amended to clarify that the host controller produces at its data out terminal an output signal comprising a serial digital data stream including MxN bits, so that the bits are "sequentially loaded into and respectively fill the positions of the (MxN)-bit register (claims 13 and 24), or to specify transmitting to the local controllers a serial digital data message including MxN bits "so that the MxN bits respectively occupy the MxN positions of the shift register" (claim 31). No such arrangement is disclosed or suggested by any of the cited references.

In Acres et al., the local controllers or microprocessors 248A-248H are coupled to a floor controller CPU by data buses, and each microprocessor has two serial signal lines 251 which are, respectively, coupled to current loop networks through a current loop driver 250, each such current loop network in turn including a plurality of control gaming devices (Fig. 12). The microprocessors 248A-248H do not form a shift register, nor does Acres et al. disclose a serial digital data stream including bits equal in number to the positions in the shift register and to the devices being accessed, nor is any such arrangement disclosed or suggested by the other references. Rather, the references describe systems which operate in an entirely different manner. Accordingly, it is believed that each of the independent claims 13, 24 and 31 and the claims dependent thereon, as amended, clearly patentably distinguish from the cited art.

Additionally, it is noted that each of the independent claims specifies an arrangement wherein "each local controller having its device terminals respectively connected to individual ones of the devices" (claims 1 and 5), or wherein each local controller includes a shift register "with the register positions respectively connected to device output terminals to which the devices of the associated node may respectively be connected" (claims 13 and 24), or grouping of the devices so that each node includes a local controller "forming a M-bit shift register and up to M devices respectively connected to device terminals respectively connected to the register positions of the local controller" (claim 31). No such arrangement is disclosed or suggested by the cited references.

As was indicated above, the Acres et al. patent, which is the only reference disclosing a specific interconnection arrangement in its Fig. 12, does not have microprocessors or local controllers with device terminals respectively corresponding to and respectively connected to the devices being controlled. Rather, each microprocessor is connected via two serial signal lines and a current loop driver to a plurality of current loop networks, wherein each such current loop network includes a plurality of the controlled gaming machines. Thus, this affords an additional reason for the allowance of claims 1-36.

For all of the foregoing reasons, it is respectively submitted that, as amended, each of the claims 1-36 now patentably distinguishes from the cited references and, accordingly, allowance of those claims is respectfully asked.

Respectfully submitted,

SEYFARTH SHAW LLP

Garrettson Ellis
Registration No. 22,792
Attorney for Applicants

SEYFARTH SHAW LLP
131 So. Dearborn Street, Suite 2400
Chicago, Illinois 60603
(312) 460-5518

**Certificate of Facsimile**

I hereby certify that this correspondence is being sent Via Facsimile to the U.S. Patent and Trademark Office (Fax No. 571-273-8300) on January 17, 2007.

Registered Attorney for Applicant
Date: January 17, 2007